8.4 An 11k-Electrode 126-Channel High-Density Microelectrode Array to Interact with Electrogenic Cells

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We report on a CMOS-based microelectrode array (MEA) featuring 11,016 metal electrodes and 126 channels, each of which comprises recording and stimulation electronics, for extracellular bidirectional communication with electrogenic cells, such as neurons or cardiomyocytes. The important features include: (i) high spatial resolution at the (sub)cellular level with 3,200 electrodes per mm^2 (diameter 7μm, pitch 18μm); (ii) a reconfigurable routing of the recording sites to the 126 channels; and (iii) low noise levels.

In many experiments with living tissue it is desirable to adapt the locations of the recording sites to the biological structure [1]. One possibility is to simultaneously record from all electrodes of a HD array [2,3], which results in rather high noise levels because of the limited pixel area (e.g., 8μm pitch, 280μV$_{rms}$ noise [4]). Instead of scanning the entire electrode array, the approach presented here provides a reconfigurable routing for an almost arbitrary set of electrodes to the readout channels, and enables low-noise signal amplification and filtering, with the front-end circuit placed outside the array. The flexibility in electrode selection is attained by use of an analog switch matrix integrated underneath the electrode array. The switch matrix consists of 13k SRAM cells and analog switches (PMOS, W/L = 4/0.6) to define the routing from the electrodes to the amplifiers as illustrated in Fig. 8.4.1. To obtain the settings of the switches for a configuration, the switch matrix is represented as a graph, and a max-flow, min-cost optimization problem is solved using an integer-linear program (ILP). Arcs from spots of interest to a set of electrodes are assigned a cost, such as the Euclidian distance to the center of the spots. Simulations for the task of routing 126 randomly distributed spots of interest to the 126 channels were carried out to assess the ability to select spots of interest. The average distance from any spot of interest to its closest electrode was 6.75μm for the set used (n = 2000). The routing scheme implemented provides an average distance to the connected electrode of 7.1μm, whereas 114.6 of the 126 spots can be read out via the closest electrode. 102 electrodes in a 6×17 rectangular configuration constitute the largest obtainable coherent electrode block.

For recording, the signals are amplified and filtered using three stages, each built with a Miller-compensated amplifier (Fig. 8.4.2). The gain is programmable via the digital interface from 0 to 80dB in 18 steps to account for the large variation in the signal amplitudes of different cell types. The maximum gain of the first stage is 29.5dB. This stage also provides a first-order HPF featuring a low cut-off frequency given by the capacitance C_1 (150fF) and the two diode-connected transistors D_1 and D_2 used as resistors [5]. The low cut-off frequency is needed to reject the large DC offsets and fluctuations of the electrode-solution interface. The first stage has a measured high-pass frequency of 0.3Hz. Its bandwidth is limited with the Miller capacitance to either 15 or 50kHz. The second stage further reduces the bandwidth to 4 or 14kHz. The signals are multiplexed after the second stage, sampled at 20kHz and digitalized with 16 8b successive-approximation ADCs. The data can be oversampled at up to 160kHz by skipping channels. The data are transferred off chip along with the chip-status and a CRC. The stimulation capability is provided through an 8b flash DAC and stimulation buffers. Additional channels are used to record the on-chip temperature and the electrode DC potential.

To electrically characterize the chip, probe switches driven by a shift-register are integrated that allow for automated analog testing. The measured transfer function is shown in Fig. 8.4.3. The lower part shows the noise spectrum of (i) the amplifiers (2.4μV$_{rms}$ equivalent-input noise, 1Hz to 100kHz), (ii) with blank Pt-electrodes (3.9μV$_{rms}$) and (iii) with dendritic Pt-black electrodes (3.0μV$_{rms}$) in saline solution. Compared to [6], noise is reduced by 10dB, which is mainly due to the use of the diodes $D_{1,2}$ and the relaxed area constraints (i.e., larger input transistors). Additionally, the ADC contributes 0.5LSB quantization noise. Worst-case signal crosstalk within the array was assessed to be 67dB in a saline solution using Pt-black electrodes. The standard deviation of the input-referred offset is 0.7mV, which will be improved using an offset compensation scheme in a redesign. Currently, channels that are within range are identified, and only those are routed to the electrodes. The overall chip power consumption is 135mW, 115mW of which is consumed by the 3rd stage, the ADCs and the digital core located more than 2mm away from the array (Fig. 8.4.7). The power dissipation within the array itself is negligible. One readout channel (stage 1, 2) consumes 160μW in an area of 0.07mm^2.

A custom-designed PCB was built as shown in Fig. 8.4.4. It provides sockets for 5 neurochips that can be operated simultaneously. It is essential to avoid mechanical perturbation by handling devices with plated cells prior to measurements so that a multichip setup has been developed [7]. The data from the 5 devices are multiplexed to a single LVDS twisted pair and sent to an FPGA board at a rate of 16MB/s. The FPGA provides data processing features, such as CRC error detection, digital filtering, event detection and data reduction/compression. The preprocessed data are sent to a PC for further data processing, visualization and storage [8].

The chip was fabricated in an industrial 0.6μm 3M2P CMOS-process, the electrodes are fabricated using post-processing steps. Ti:W (20nm) and platinum (200nm) as electrode materials were sputtered onto the wafer and patterned using a lift-off process. A 1.6μm thick passivation layer stack (SiO_2 and Si_3N_4) was deposited for corrosion protection [6]. The Pt electrode openings were shifted away from the locations of the original CMOS aluminum contacts to ensure long-term stability. Figure 8.4.5 shows the fabricated chip, on which chicken dorsal root ganglion neurons have been cultured for 2 days *in vitro* (DIV). The inset illustrates the shifted electrode design.

Figure 8.4.6 shows spontaneous activity from biological preparations obtained with the HD MEA to illustrate the broad range of applications. The top trace was obtained from neonatal rat cardiomyocytes (3DIV). The middle trace stems from dissociated rat hippocampal neurons cultured for 16DIV. The two traces at the bottom are obtained from a Long-Evans rat acute brain slice preparation [9]. The two electrodes are located at a distance of 38μm.

Acknowledgements:
The authors would like to thank Dr. U. Egert, C. Diaz, E. Perriard, T. Ugniwenko, Dr. A. Blau, Dr. B. Roscic for help with the biological measurements, the EMZ, University Zurich for Fig. 8.4.5 and Prof. Henry Baltes for sharing laboratory resources and for his ongoing interest in their work.

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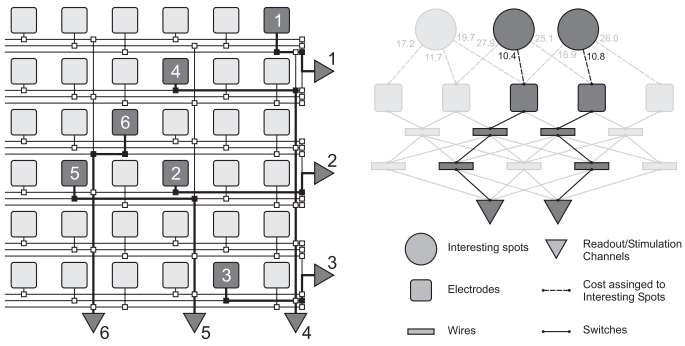

Figure 8.4.1: Array wiring and routing scheme.

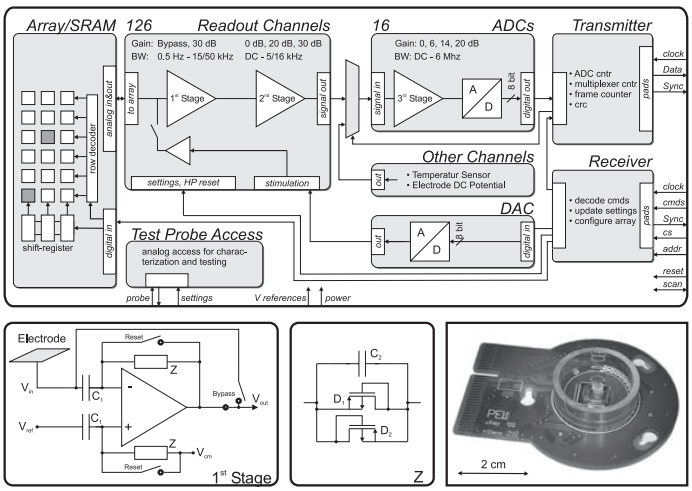

Figure 8.4.2: Chip block diagram and 1st stage schematics.

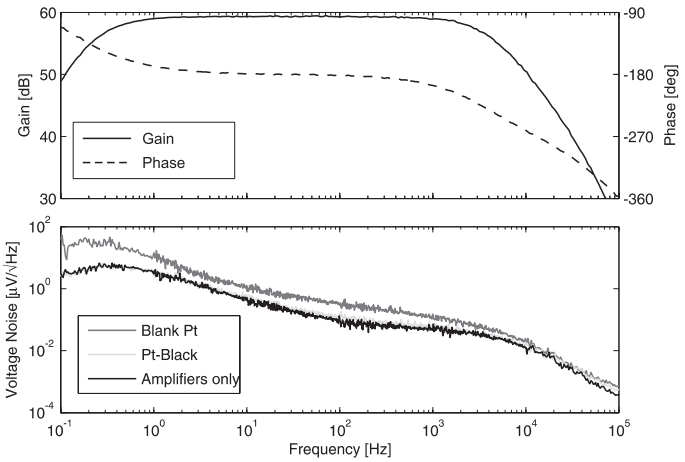

Figure 8.4.3: Measured transfer function, noise spectrum.

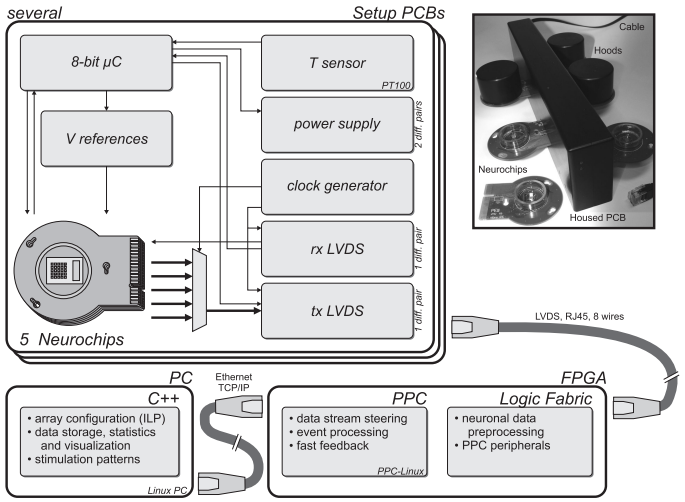

Figure 8.4.4: Measurement setup.

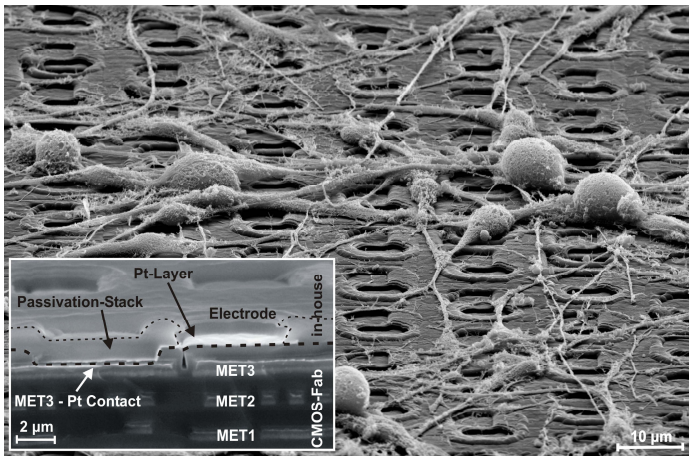

Figure 8.4.5: SEM with neurons, chip cross-section.

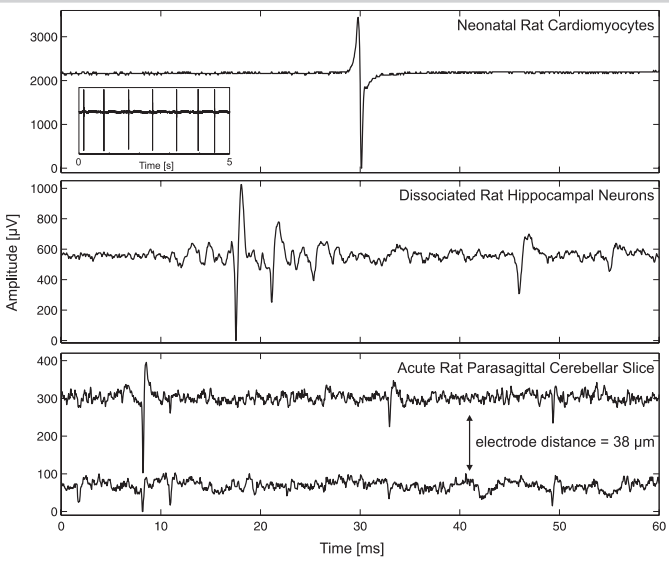

Figure 8.4.6: Biological measurements.

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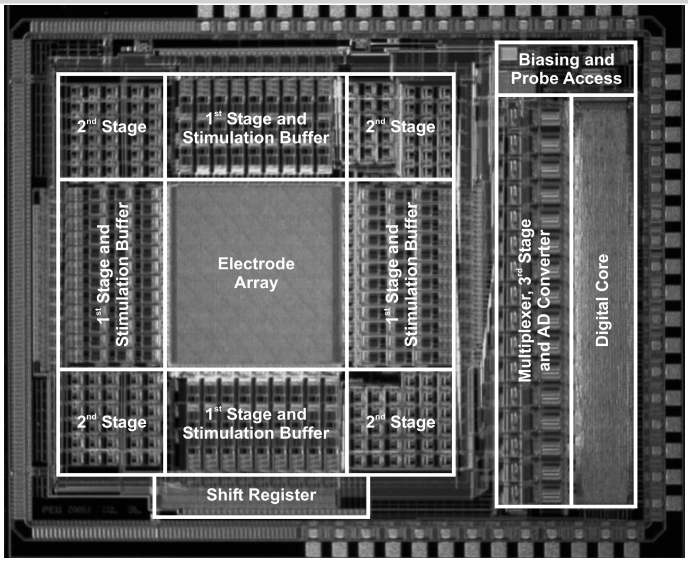

Figure 8.4.7: Chip micrograph.

